CLAIMS

What is claimed is:

1. A signal processor having a re-configurable logic circuitry that operates on a plurality of data, the signal processor comprising:

a configuration control circuitry that selects at least one logic configuration that is used to program the re-configurable logic circuitry; and

a programmable logic configuration circuitry comprising an active configuration circuitry and a loading configuration circuitry, the loading configuration circuitry receives at least one additional logic configuration, and the active configuration circuitry programs the re-configurable logic circuitry using the at least one logic configuration.

2. The signal processor of claim 1, wherein the re-configurable logic circuitry further comprises:

a data memory, a data addressing unit, an arithmetic logic unit, and an instruction decode and sequencing unit; and

wherein each of the data memory, the data addressing unit, the arithmetic logic unit, and the instruction decode and sequencing unit is communicatively coupled to the programmable logic configuration circuitry and is independently programmable using the programmable logic configuration circuitry.

3. The signal processor of claim 1, wherein the signal processor employs a wide word width to program the re-configurable logic circuitry, the wide word width is operable to configure an entirety of the re-configurable logic circuitry.

4. The signal processor of claim 1, wherein the re-configurable logic circuitry is partitioned into a plurality of areas, each area within the plurality of areas is independently programmable.

5. The signal processor of claim 1, wherein the programmable logic configuration circuitry loads a default logic configuration into the re-configurable logic circuitry.

6. The signal processor of claim 5, wherein the default logic configuration is stored in a memory.

7. The signal processor of claim 1, wherein configuration control circuitry generates an adaptive logic configuration.

8. The signal processor of claim 7, wherein the adaptive logic configuration is generated using a processing circuitry.

9. The signal processor of claim 7, further comprising a data monitoring circuitry that generates the adaptive logic configuration in response to at least one characteristic of the plurality of data.

10. A signal processor having a programmable logic circuitry that operates on a plurality of data, the signal processor comprising:

the programmable logic circuitry; and

a programmable logic configuration circuitry that provides a logic configuration to the programmable logic circuitry.

11. The signal processor of claim 10, wherein the signal processor employs a wide word width to program the programmable logic circuitry, the wide word width is operable to configure an entirety of the programmable logic circuitry.

12. The signal processor of claim 10, wherein the programmable logic configuration circuitry further comprises:

a default configuration circuitry; and

an adaptive configuration circuitry.

13. The signal processor of claim 12, wherein the default configuration circuitry contains a default logic configuration for the programmable logic circuitry.

14. The signal processor of claim 12, wherein the adaptive configuration circuitry generates an adaptive logic configuration for the programmable logic circuitry.

15. The signal processor of claim 10, wherein the programmable logic circuitry is partitioned into a plurality of areas, each area within the plurality of areas is independently programmable

16. A method that provides a logic configuration to a programmable logic circuitry comprising:

selecting the logic configuration;

programming a logic array circuitry using the logic configuration; and

the logic configuration is selected based upon at least one characteristic of a plurality of data.

17. The method of claim 16, further comprising selecting an alternative logic configuration.

18. The method of claim 16, wherein the logic configuration is a default logic configuration.

19. The method of claim 16, wherein the logic configuration is an adaptive logic configuration.

20. The method of claim 16, wherein the logic configuration is provided to the logic array circuitry via a wide word width, the wide word width is operable to configure an entirety of the logic array circuitry.